

FIGURE 1

100

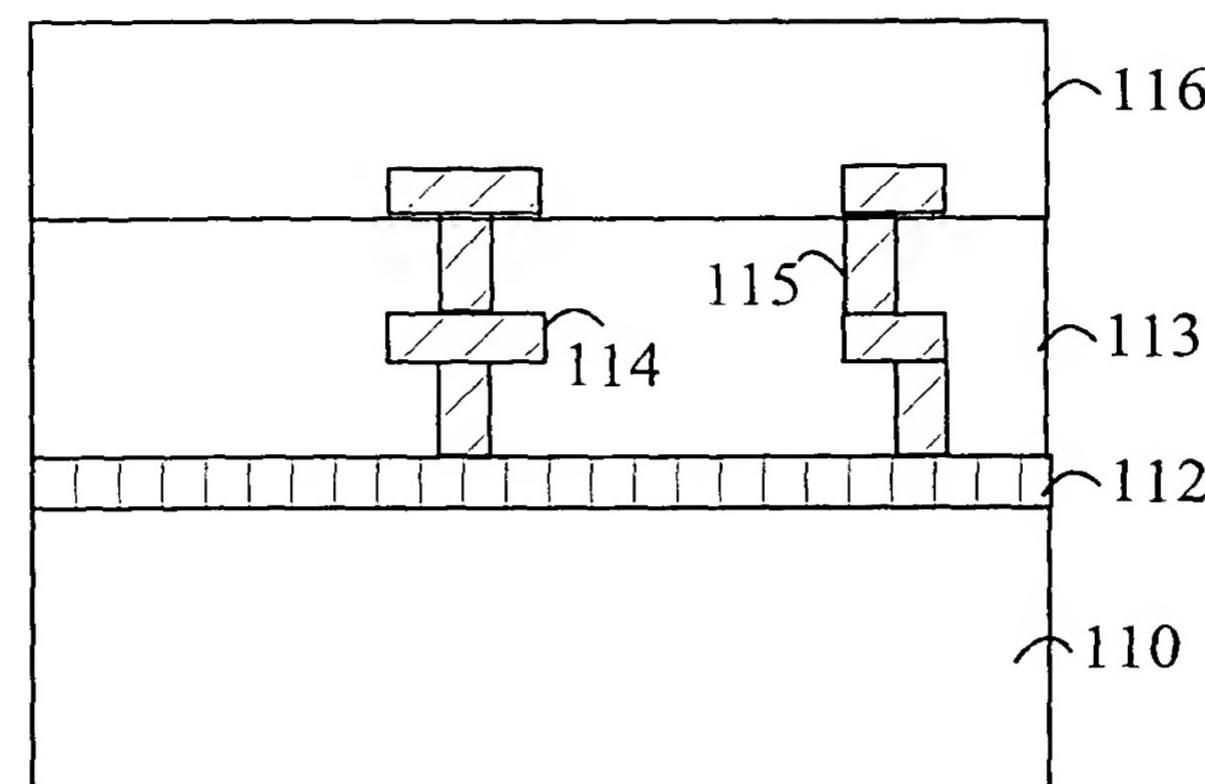


FIGURE 2

120

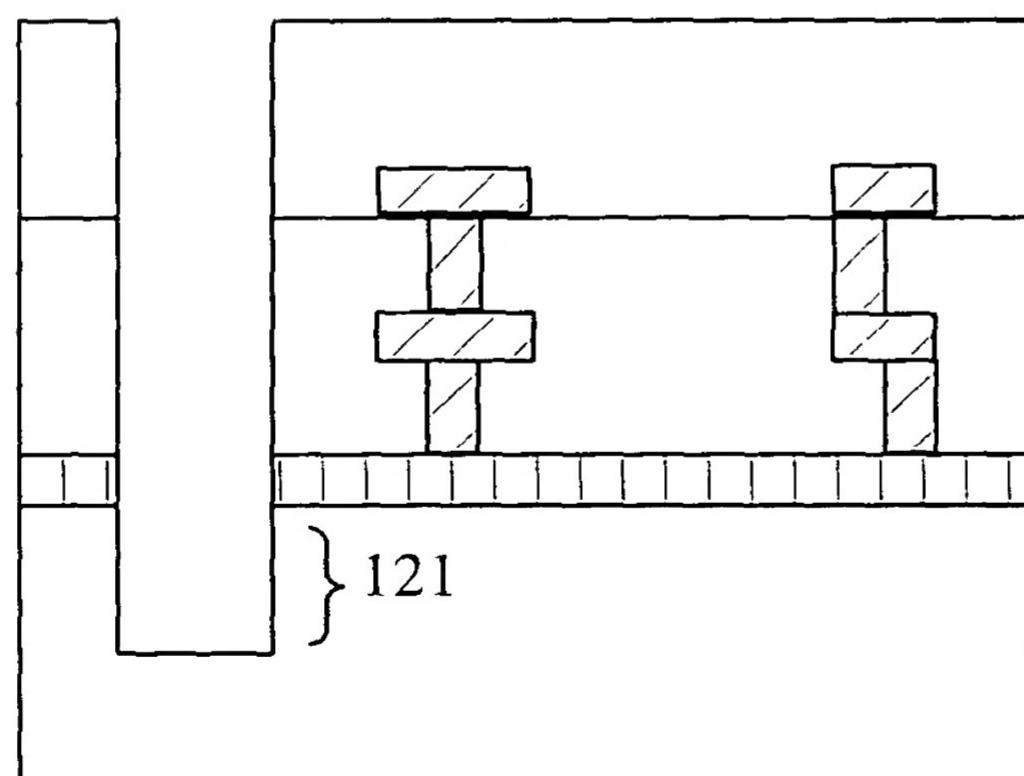


FIGURE 3

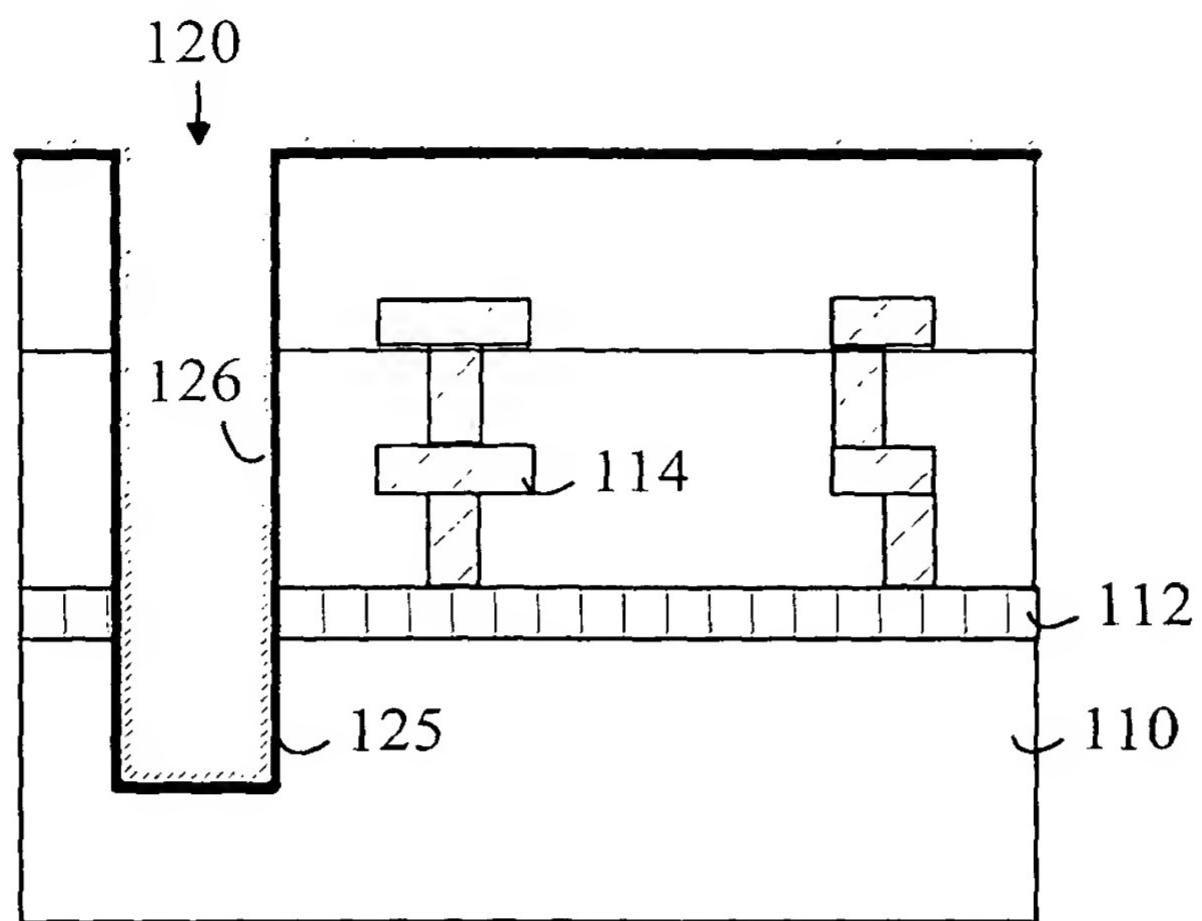


FIGURE 4

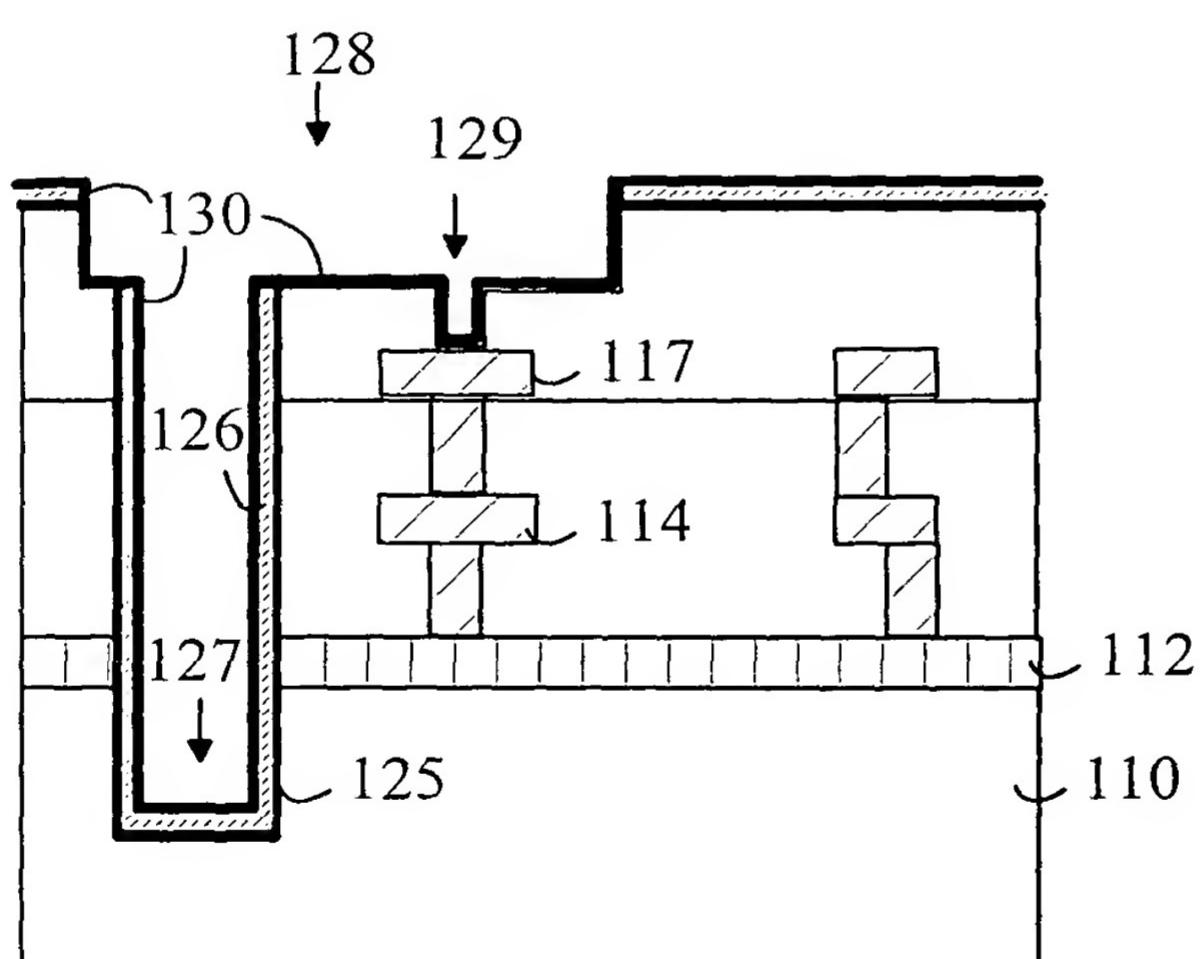


FIGURE 5

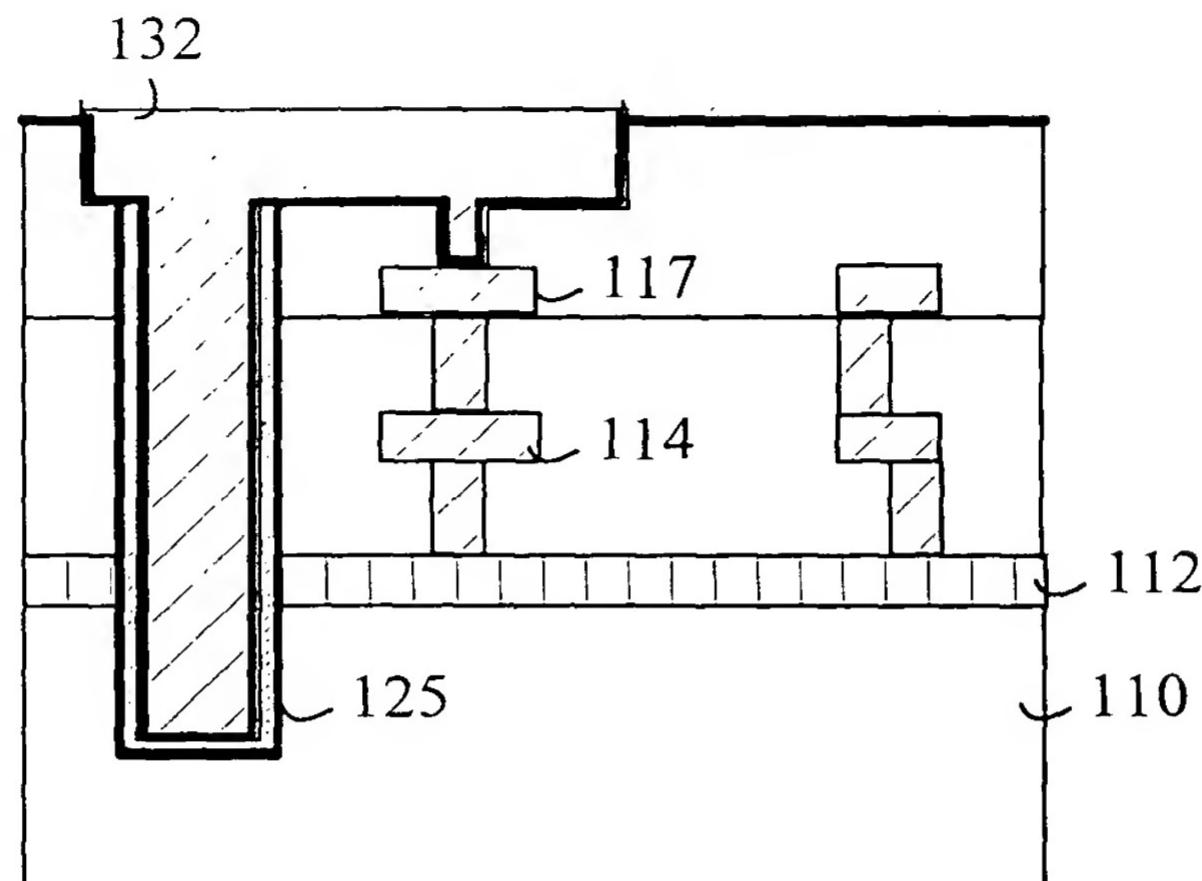


FIGURE 6

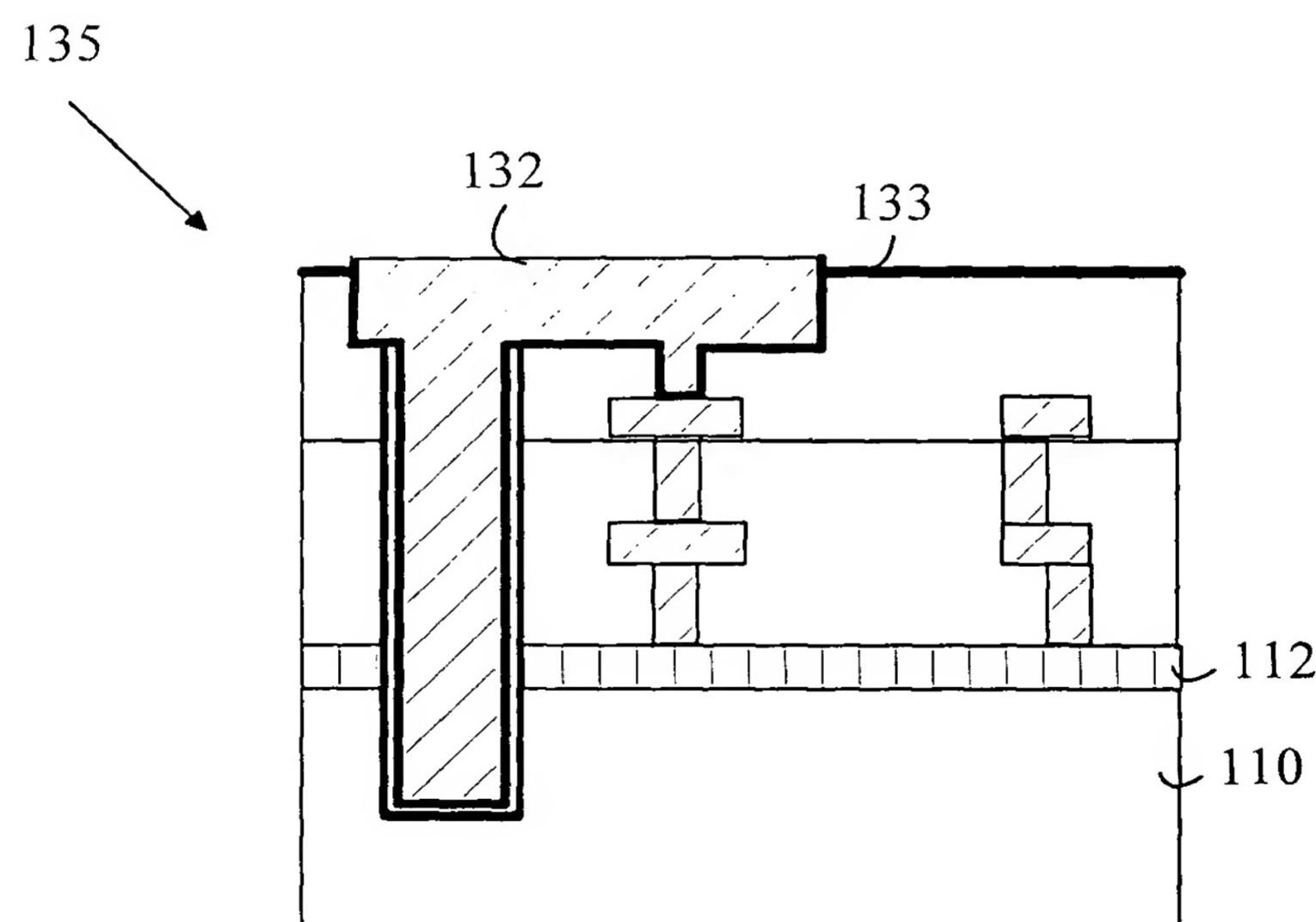


FIGURE 7

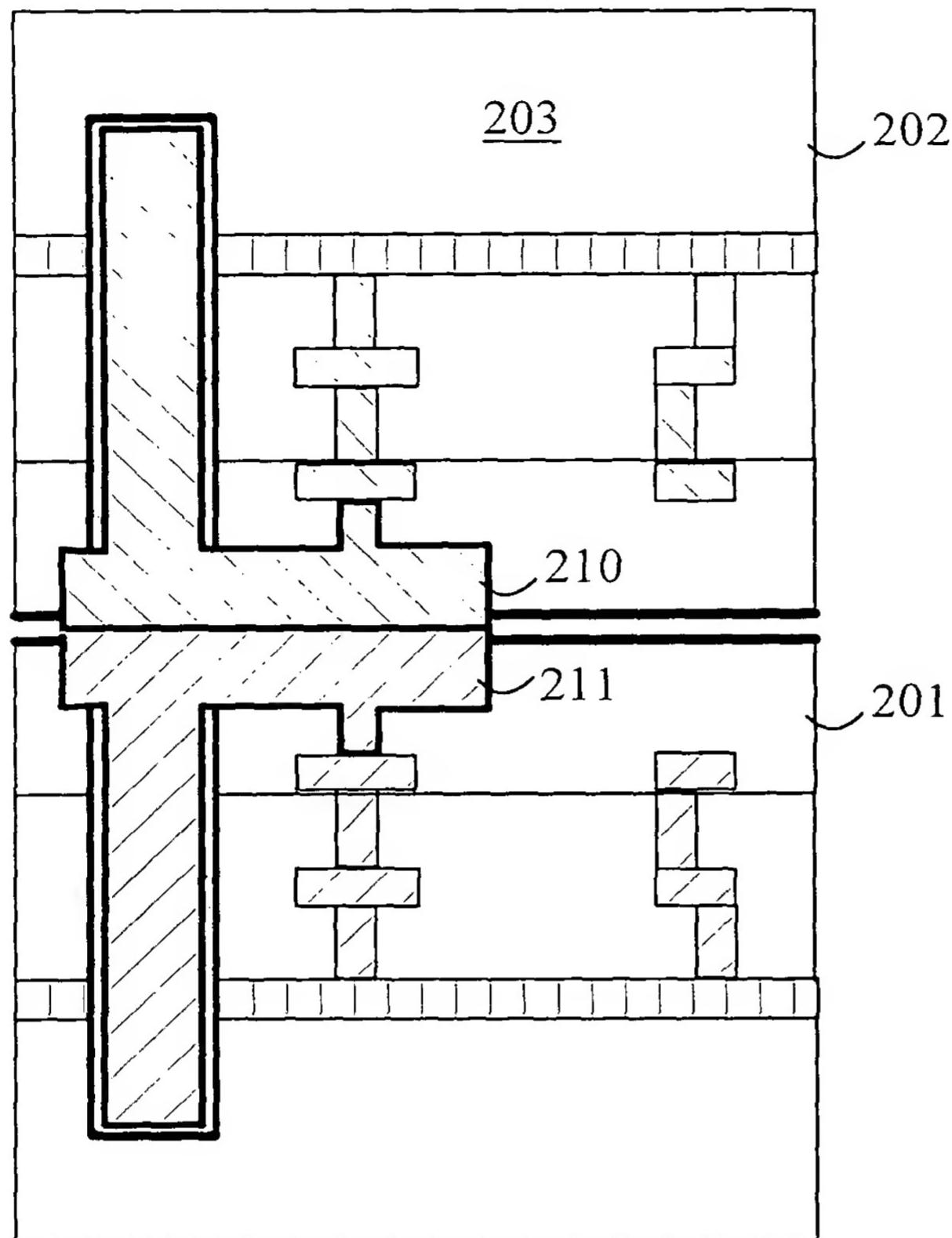


FIGURE 8

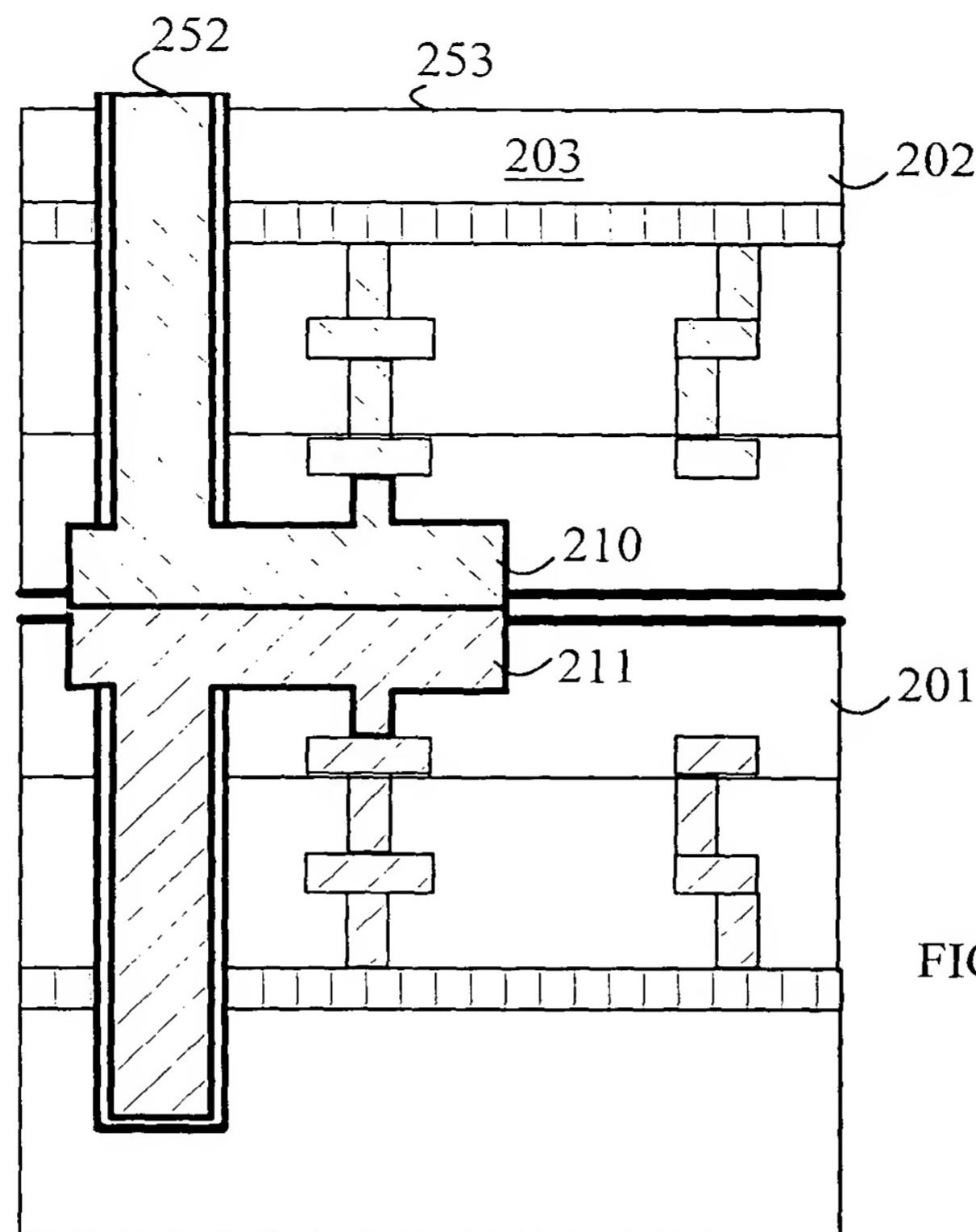


FIGURE 9

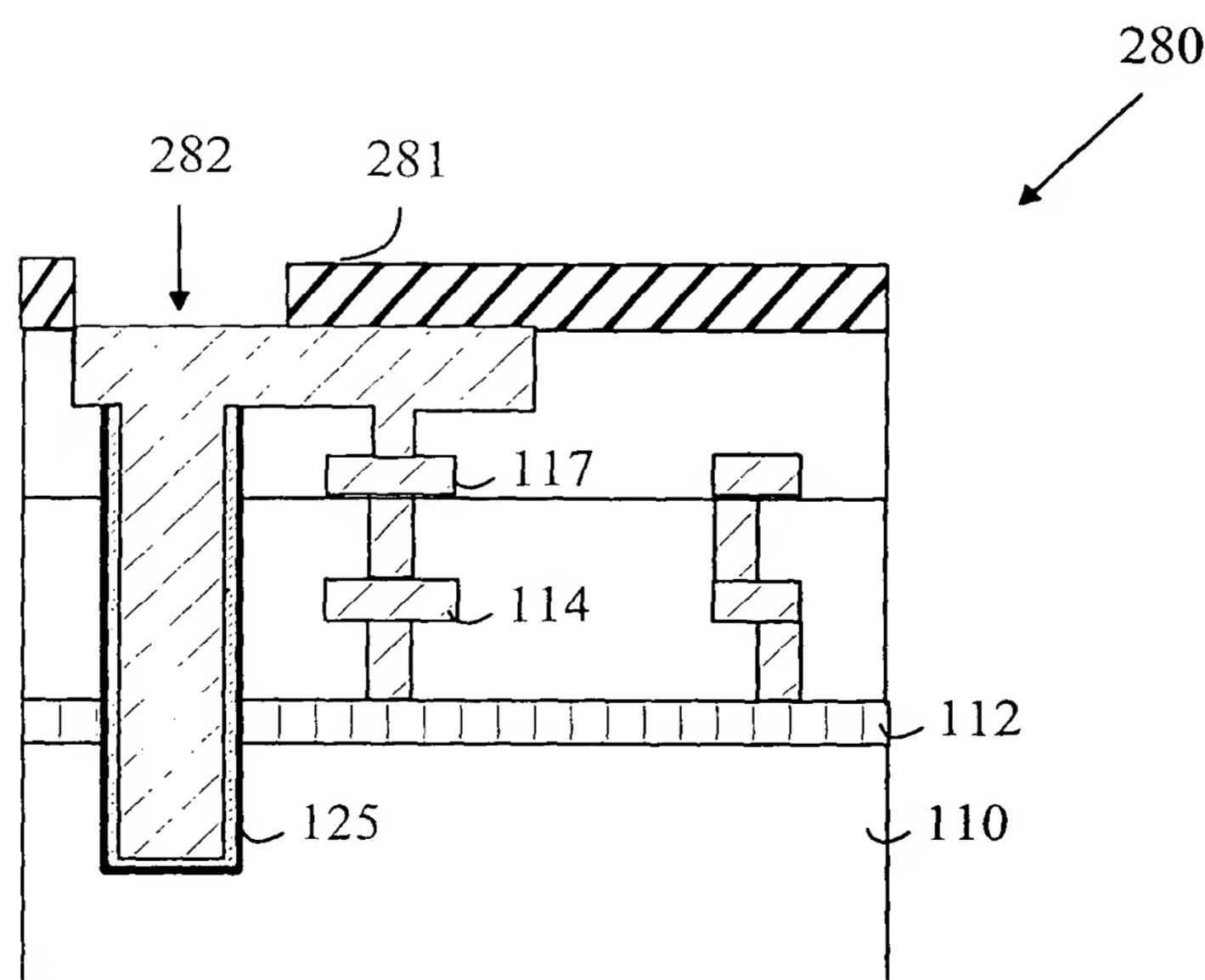


FIGURE 10

Interlocking Conductor Method for Bonding Wafers to Produce Stacked Integrated Circuits

Inventor: Patti

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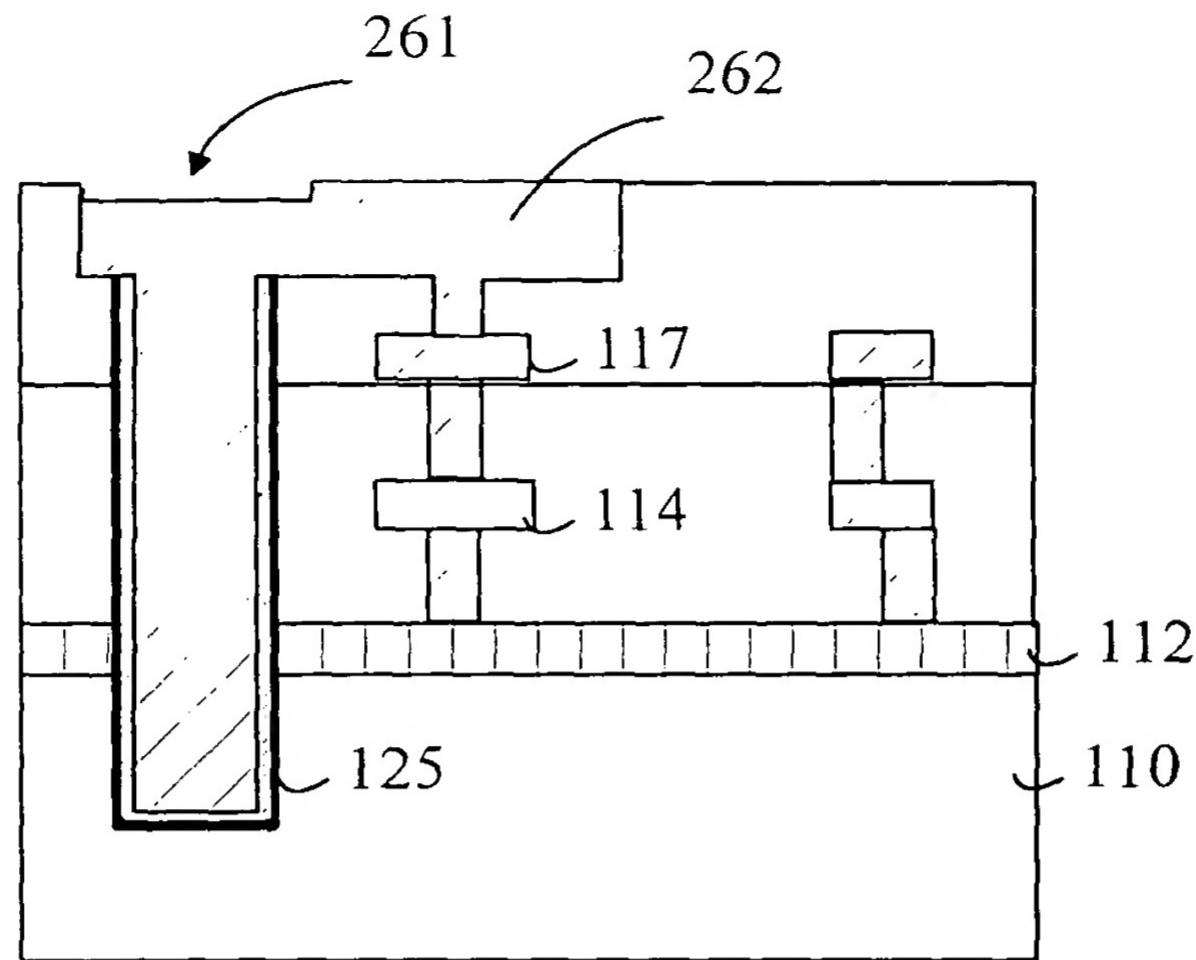


FIGURE 11

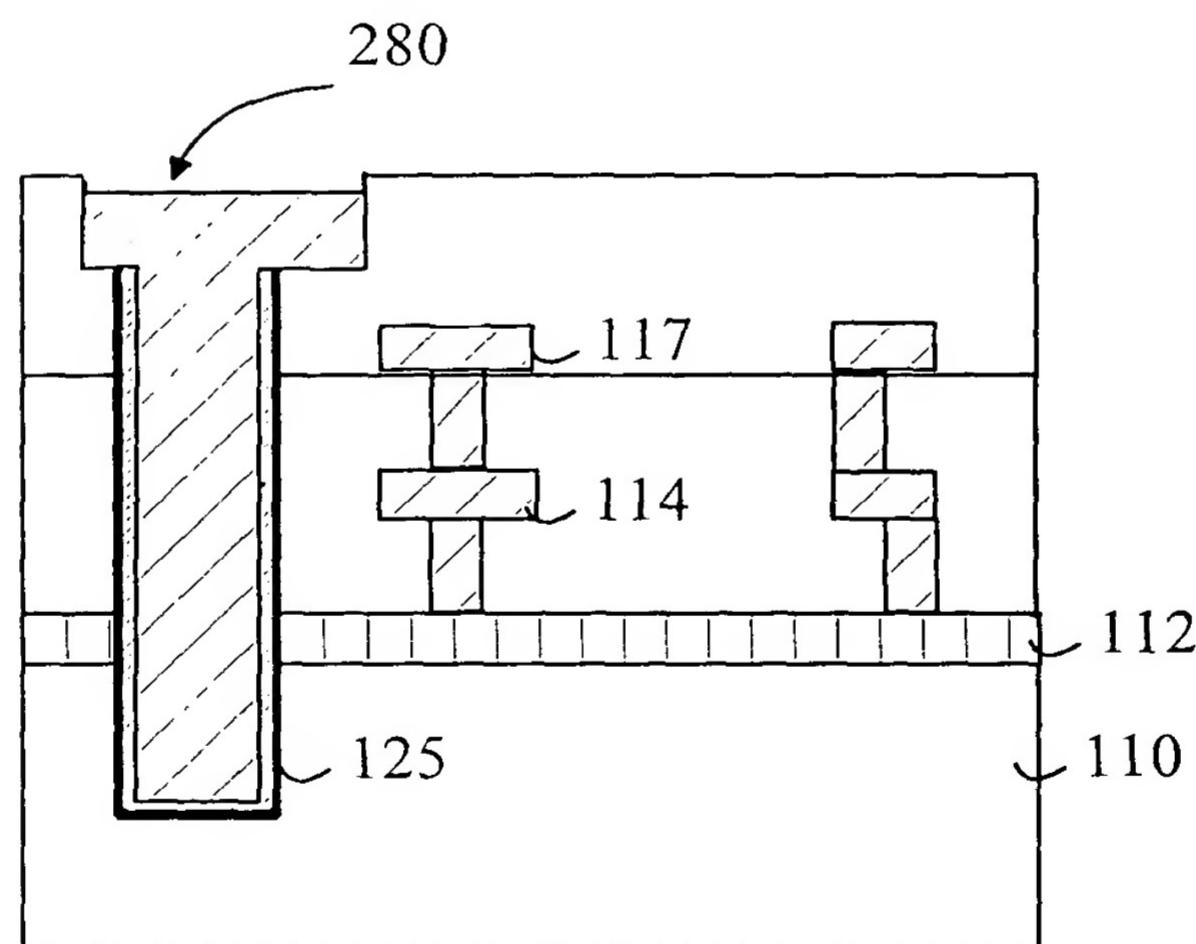


FIGURE 12